3. (Twice Amended) A [bipolar] transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one drain region and said at least one source region on said at least one active area;

a first barrier layer substantially covering said at least one field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through [a] <u>said</u> first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one drain region on said semiconductor substrate;

at least one source contact plug extending through [a] <u>said</u> first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one source region on said semiconductor substrate;

at least one drain contact land disposed atop said at least one drain contact plug, wherein said at least one drain contact land [has a larger cross-sectional area] <u>is wider</u> than said at least one drain contact plug <u>and is substantially planar</u>;

at least one source contact land disposed atop said at least one source contact plug, wherein said at least one source contact land [has a larger cross-sectional area] <u>is wider</u> than said at least one source contact plug <u>and is substantially planar</u>;

a second barrier layer disposed over said first barrier layer;

at least one upper source contact extending through said second barrier layer, wherein said at least one upper source contact is in electrical communication with said at least one source contact land; and

at least one upper drain contact extending through said second barrier layer, wherein said at least one upper drain contact is in electrical communication with said at least one drain contact land.

4. (Amended) The [bipolar] transistor of claim 3 further comprising drain contact metallization in electrical communication with said at least one upper drain contact; and source contact metallization in electrical communication with said at least one upper source contact.

5. (Twice Amended) The [bipolar] transistor of claim 3, wherein said at least one source contact plug extends between at least two source regions.

6. (Twice Amended) The [bipolar] transistor of claim 3, wherein said at least one drain contact plug extends between at least two drain regions.

7. (Twice Amended) The [bipolar] transistor of claim 3, wherein said at least one source contact land extends between at least two source contact plugs.

8. (Twice Amended) The [bipolar] transistor of claim 3, wherein said at least one drain contact land extends between at least two drain contact plugs.

9. (Twice Amended) The [bipolar] transistor of claim 3, wherein said at least one upper source contact extends between at least two source contact lands.

10. (Twice Amended) The [bipolar] transistor of claim 3, wherein said at least one upper drain contact extends between at least two drain contact lands.

19. (Amended) A semiconductor device including at least one contact, comprising:

a contact plug extending through a first barrier layer, wherein said contact plug is in electrical communication with an active region on a semiconductor substrate;

a contact land disposed atop said contact plug, wherein said contact land [has a larger cross-sectional area] is wider than said contact plug and is substantially planar;

an upper contact extending through a second barrier layer, which is disposed over said first barrier layer, to form an electrical contact with said contact land.

21. (Twice Amended) A semiconductor device including at least one [bipolar] transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a semiconductor substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

a first barrier layer substantially covering said at least one thick field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through said first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one implanted drain region on said semiconductor substrate;

at least one source contact plug extending through said first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one implanted source region on said semiconductor substrate;

at least one drain contact land disposed atop said at least one drain contact plug, wherein said at least one drain contact land [has a larger cross-sectional area] is wider than said at least one drain contact plug;